

In the Claims:

Claim 1 (currently amended): A floating gate memory cell situated on a substrate, said floating gate memory cell comprising:

a stacked gate structure situated on said substrate, said stacked gate structure being situated over a channel region in said substrate;

a recess formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth;

a source of said floating gate memory cell situated adjacent to said sidewall of said recess and under said stacked gate structure;

a Vss connection region situated under said bottom of said recess and under said source, said Vss connection region being connected to said source, said Vss connection region being a heavily doped region to reduce a Vss resistance;

wherein said Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region, thereby preventing an increase in a drain induced barrier lowering.

Claim 2 (original): The floating gate memory cell of claim 1 wherein said reduced lateral diffusion of said source causes a reduction in drain induced barrier lowering in said floating gate memory cell.

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Claim 3 (canceled)

Claim 4 (original): The floating gate memory cell of claim 1 wherein said sidewall of said recess is substantially perpendicular to a top surface of said substrate.

Claim 5 (original): The floating gate memory cell of claim 1 wherein said depth of said recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms.

Claim 6 (original): The floating gate memory cell of claim 1 wherein said stacked gate structure comprises an ONO stack situated on a floating gate.

Claim 7 (original): The floating gate memory cell of claim 1 wherein said floating gate memory cell is a NOR-type floating gate flash memory cell.

Claim 8 (currently amended): A floating gate memory cell situated on a substrate, said floating gate memory cell comprising a stacked gate structure situated on said substrate, said stacked gate structure being situated over a channel region in said substrate, a recess formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth, said floating gate memory cell being characterized in that:

a source of said floating gate memory cell is situated adjacent to said sidewall of said recess and under said stacked gate structure, a Vss connection region is situated under said

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bottom of said recess and under said source, said Vss connection region being connected to said source, said Vss connection region being a heavily doped region to reduce a Vss resistance, wherein said Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region, thereby preventing an increase in a drain induced barrier lowering.

Claim 9 (original): The floating gate memory cell of claim 8 wherein said reduced lateral diffusion of said source causes a reduction in drain induced barrier lowering in said floating gate memory cell.

Claim 10 (canceled)

Claim 11 (original): The floating gate memory cell of claim 8 wherein said sidewall of said recess is substantially perpendicular to a top surface of said substrate.

Claim 12 (original): The floating gate memory cell of claim 8 wherein said depth of said recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms.

Claim 13 (original): The floating gate memory cell of claim 8 wherein said stacked gate structure comprises an ONO stack situated on a floating gate.

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Claim 14 (original): The floating gate memory cell of claim 8 wherein said floating gate memory cell is a NOR-type floating gate flash memory cell.

Claims 15-20 (canceled)